UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,761	02/20/2004	Sungdo Moon	200313044-1	7412

22879 7590 01/22/2007
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
WANG, BEN C	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,761	MOON ET AL.	
	Examiner	Art Unit	
	Ben C. Wang	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application and presented for examination.

Claim Rejections – 35 USC § 102(b)

2. The following is a quotation of 35 U.S.C. 102(b) which forms the basis for all obviousness rejections set forth in this office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being unpatentable over Ayers et al. (hereafter 'Ayers') (Aggressive Inlining, 1997, ACM).

4. **As to claim 1**, Ayers discloses a method for cross-module in-lining (Sec. 1, 4th Para., Lines 7-9), comprising:

In a first phase of a compiling process, deciding to in-line a first function in a first module into a second function in a second module (Fig. 4 - screen inline candidates & select inline sites; Sec. 2.4, 3rd Para., Lines 1-2, 5-17); providing the location of the first function (Sec. 2.4, 1st Para, Lines 1-2; Sec. 2.3, 6th Para., Lines 7-13 – the address of a file-static procedure); providing instructions for in-lining to be performed in a second phase of the compiling process (Sec. 2.2, 1st Para., Lines 1-4, 6-9; Sec. 2.1, 1st Para., Lines 4-8);

In the second phase of the compiling process, following the instructions to in-line code of the first function into the second function (Sec. 2.2, 1st Para., Lines 9-12).

5. **As to claim 10**, Ayers discloses a method for compiling a first set of modules having programming source code (Fig 1 (bottom), element – Sources), comprising:

In a first phase (Fig. 1 (bottom), elements - Sources, Front End), from the first set of modules, providing a second set of modules having first intermediate representations (Sec. 2.1, 1st Para., Lines 1-4);

In a second phase (Fig. 1 (bottom), element - Inter-procedural Optimization), performing in-line analysis on the second set of modules (Sec. 2.2, 1st Para., Lines 6-8); providing instructions for in-lining to be performed in a third phase of the compiling process (Sec. 2.2, 1st Para., Lines 9-12); and providing a third set of modules having second intermediate representations optimized (Sec. 1, 4th Para., Lines 1-3; Sec. 2.2, 1st Para., Lines 1-6, 2nd Para.) from the first intermediate representations (Sec. 2.2, 1st Para., Lines 9-12 - ucode);

In the third phase of the compiling process (Fig. 1 (bottom), element - Per-Routine Optimization), following the instructions to perform in-lining (Sec. 2.2, 1st Para., Lines 9-12), and providing a fourth set of modules (Sec. 2.2, 1st Para., Lines 9-12 – object code) having third intermediate representations optimized (Sec. 2.2, 1st Para., Lines 9-11 – ucode; 2nd Para. - optimization) from the second intermediate representations (Sec. 2.1, 1st Para., Lines 1-3 – IR – Internal Representation).

6. **As to claim 15**, Ayers discloses a computer-readable medium embodying a compiler, the compiler comprising: a front-end phase (Fig. 1 (bottom), element – Front End); a cross-module analysis phase (Fig. 1 (bottom), element – Inter-procedural Optimization); and a back-end phase (Fig. (bottom), element – Per-Routine Optimization); wherein the front-end phase invokes the cross-module analysis phase (Sec. 2, 1st Para., Lines 1-4; Fig. 1 (bottom), element - Sources) ; the cross-module analysis phase determines whether a callee is to be in-lined into a caller in the back-end phase (Fig. 4 - screen inline candidates & select inline sites; Sec. 2.4, 3rd Para., Lines 1-2, 5-17); provides instructions for the back-end phase to transform in-lining code of the callee (Sec. 2.2, 1st Para., Lines 9-12); and invokes the back-end phase (Sec. 2.1, 1st Para., Lines 4-8; and the back-end phase transforms the in-lining code based on the instructions (Sec. 2.2, 3rd Para., Lines 8-11).

7. **As to claim 2**, Ayers discloses the method wherein: the compiling process comprising a front-end phase (Fig. 1 (bottom), element – Front End), an inter-procedural analysis phase (Fig. 1 (bottom), element – Inter-procedural Optimization), and a back-end phase (Fig. (bottom), element – Per-Routine Optimization); the inter-procedural phase being the first phase (Sec. 2.2, 1st Para., Lines 1-4); and the back-end phase being the second phase (Sec. 2.2, 1st Para., Lines 9-12).

8. **As to claim 3**, Ayers discloses the method in the first phase of the compiling process, further having a third function in the module containing the second function (Sec. 2.4, 3rd Para., Lines 5-17).

9. **As to claim 4**, Ayers discloses the method in the second phase of the compiling process, further getting rid of the third function in the module containing the second function after using that third function to in-line its code into the second function (Sec. 3.2, 3rd Para., Lines 6-10).

10. **As to claim 5**, Ayers discloses the method wherein the third function being selected from a group (Sec. 1, 4th Para., Lines 1-3) consisting of the first function (Sec. 1, 2nd Para., Lines 1-3) and a clone of the first function (Sec. 1, 2nd Para., Lines 7-11).

11. **As to claim 6**, Ayers discloses the method wherein in the second phase of the compiling process, in-lining the code of the first function into the second function uses a clone of the first function (Sec. 2.3; Fig. 3).

12. **As to claim 7**, Ayers discloses the method wherein in the second phase of the compiling process, the code used to be in-lined into the second function is stored in a file (Sec. 2.1, 1st Para., Lines 8-15).

13. **As to claim 8**, Ayers discloses the method wherein in the second phase of the compiling process, the code used to be in-lined into the second function is stored in a library (Sec. 3.1, 2nd Para., Lines 1-7).

14. **As to claim 9**, Ayers discloses the method wherein the instructions include at least a list of callees to be in-lined and corresponding callers (Sec. 1, 4th Para., Lines 7-13 – it can inline or clone calls both within and across program modules).

15. **As to claim 11**, Ayers discloses the method in the second phase, further using code in the module containing a function caller of a function callee to transform in-lining (Sec. 1, 2nd Para, Lines 1-3).

16. **As to claim 12**, Ayers discloses the method wherein the code being selected from a body of the function callee (Sec. 1, 2nd Para., Lines 1-3).

17. **As to claim 13**, Ayers discloses the method wherein the code being selected from a clone of the function callee (Sec. 1, 2nd Para., Lines 7-11).

18. **As to claim 14**, Ayers discloses the method wherein the instructions include at least one of: a set of function caller including at least one function caller (Fig. 4, Lines 3, 8); a set of function callee including at least one function callee (Sec. 2.4, 2nd Para., Line

1-2); the order for transformation of in-lining (Sec. 2.4, 2nd Para., Lines 2-3; 3rd Para., Lines 1-2); the location of at least one function callee (Sec. 2.3, 6th Para., Lines 7-12); and decisions whether to keep a body of at least one function callee after in-lining transformation (Sec. 3.2, 3rd Para., Lines 6-10).

19. **As to claim 16**, Ayers discloses the computer-readable medium wherein the back-end phase further performs tasks related to in-lining (Sec. 2.2, 3rd Para., Lines 8-11).

20. **As to claim 17**, Ayers discloses the computer-readable medium wherein the tasks related to in-lining include at least deleting the callee in a module containing the caller (Sec. 3.2, 3rd Para., Lines 6-10).

21. **As to claim 18**, Ayers discloses the computer readable medium wherein transforming the in-lining code uses code of a clone of the callee (Sec. 1, 2nd Para., Lines 7-11).

22. **As to claim 19**, Ayers discloses the computer-readable medium wherein a call to the callee is in a module that does not include the callee (Sec. 1, 4th Para., Lines 7-13).

23. **As to claim 20**, Ayers discloses the computer-readable medium wherein the instructions include at least a list of callees (Sec. 2.4, 2nd Para., Line 1-2).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- M. L. Graham, Compiler With Intermediate Compiling Mechanism (Pat. No. 5,940,620).
- Bates et al., System For Partial In-Line Expansion Of Procedure Calls During Program Compilation (Pat. No. 5,701,489).

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BCW BW

December 28, 2006

N. El-Hady

NABIL M. EL-HADY
SUPERVISORY PATENT EXAMINER